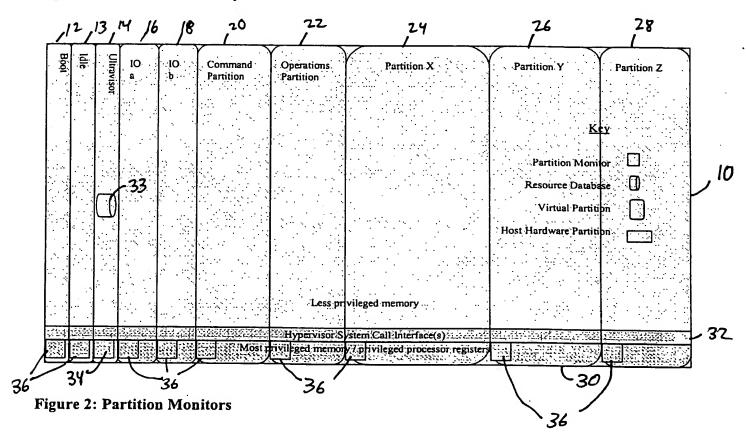
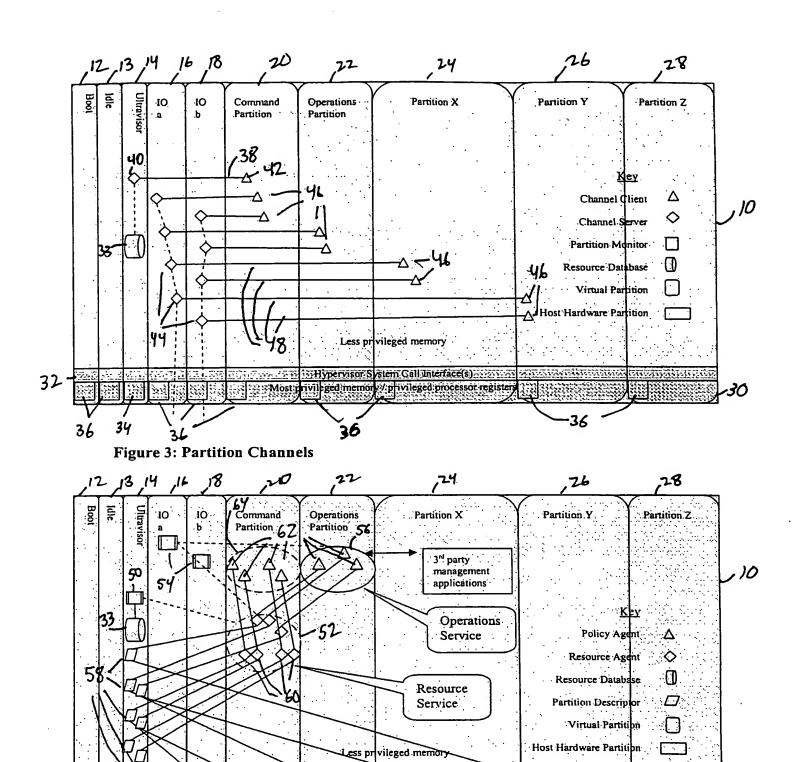


Figure 1: Partitioned Host System





Hypervisor System Call Interface(s)

Figure 4: Ultravisor Operations

ivileged memory / privileged processor register

30

## Overlapped processor throttling – default 4 bit duty width (1/16 = 6.25%)

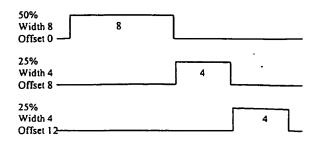


Figure 5: Processor Sharing

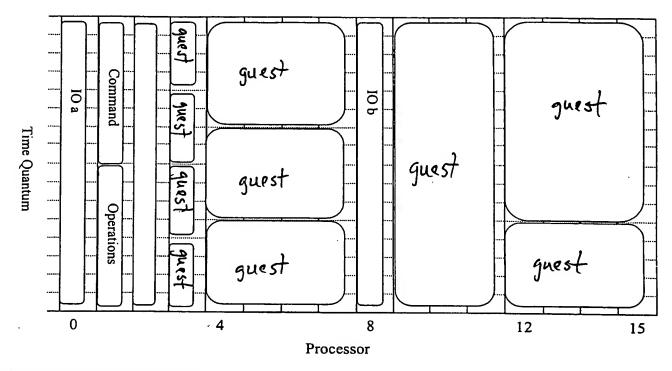


Figure 6: Processor Schedule

(2 <sup>10</sup> ) <sup>n</sup>	SI prefix	SI name	Page Table	Pageantry	1A32/EM32T
1	K	kilo	PKM	PKE	PT/PTE
2	M	mega	PMM	PME	PD/PDE
3	G	giga	PGM	PGE	PDP
4	Т	tera	PTM	PTE	PML4
5	P	peta	PPM	PPE	
6	Е	Exa	PEM	PEE	
7	Z	zetta	PZM	PZE	
8	Y	yotta	PYM	PYE	

Figure 7: SI Prefixes for Page Table Hierarchy

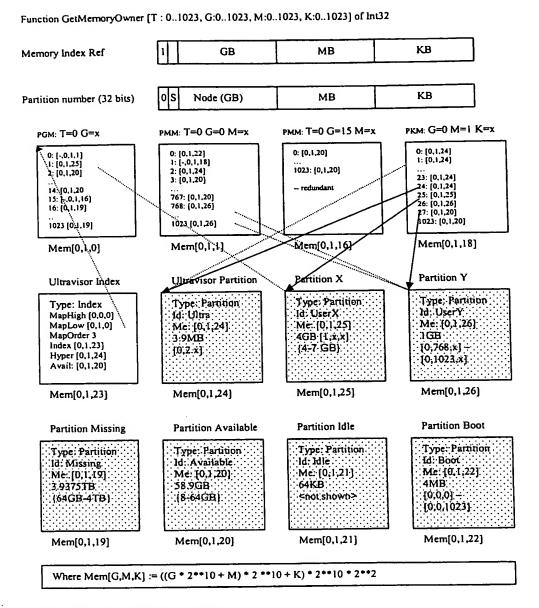
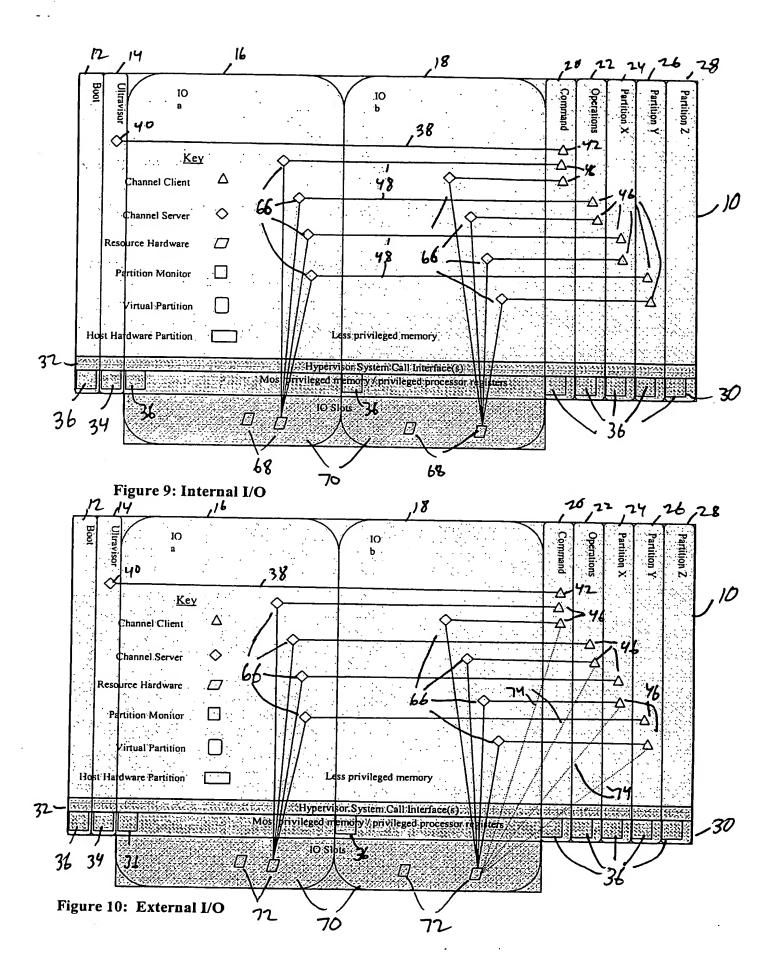


Figure 8: Partition Memory Map



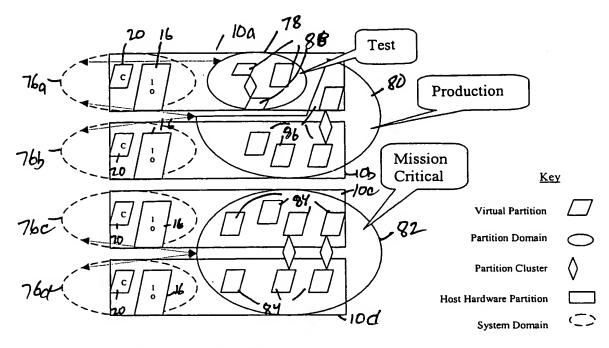


Figure 11: Ultravisor Domains

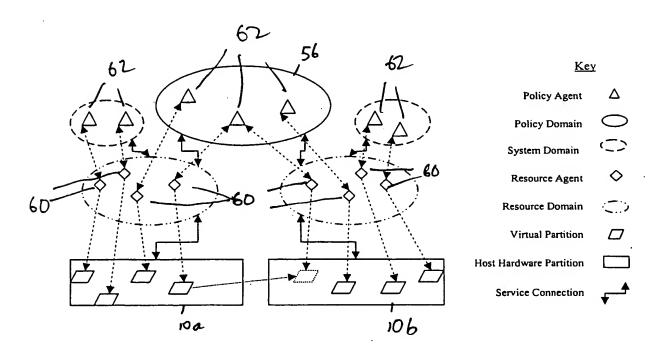


Figure 12: Ultravisor Partition Agents

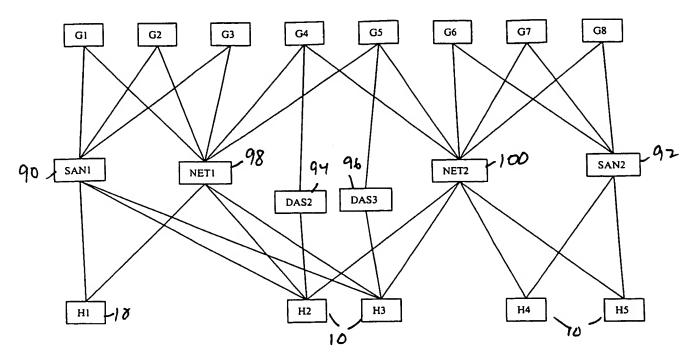


Figure 13 : Virtual Data Center Zones

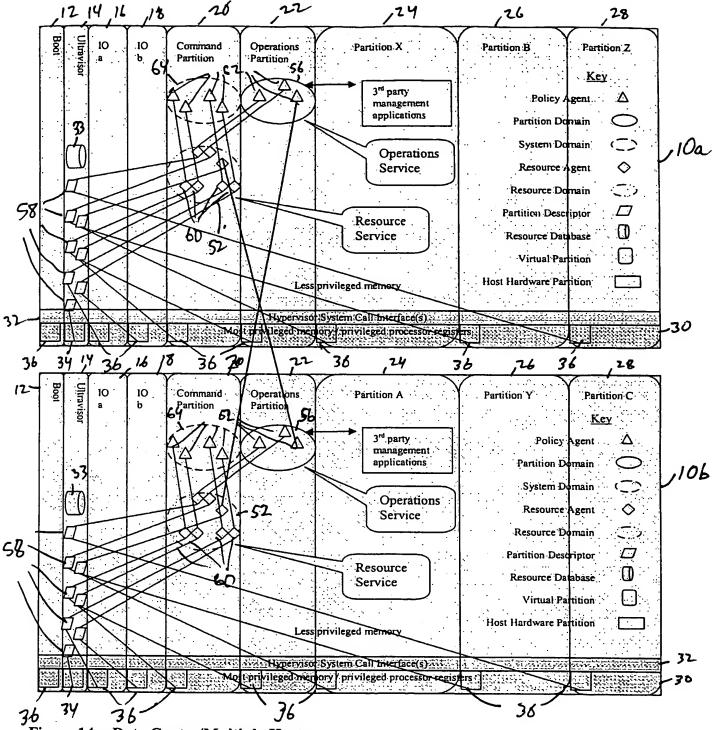
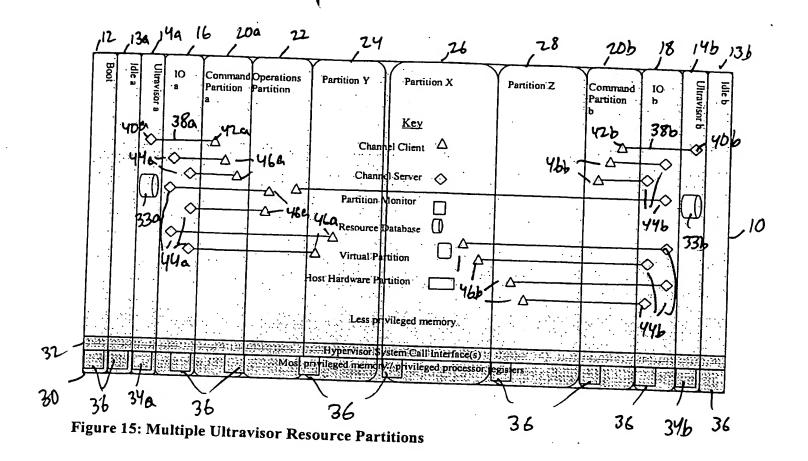


Figure 14: Data Center/Multiple Hosts



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